REMARKS

Reconsideration of the application is requested.

Applicant appreciatively acknowledges the Examiner's confirmation of receipt of applicant's claim for priority under 35 U.S.C. § 119(a)-(d).

Claims 1-20 remain in the application. Claims 1-20 are subject to examination.

Under the heading "Claim Rejections - 35 USC § 103" on pages 3-7 of the above-identified Office Action, claims 1-6, 8, 11-15, 18 and 20 have been rejected as being obvious over U.S. Patent No. 4,405,980 to Hess (hereinafter Hess) in view of U.S. Patent No. 5,150,471 to Tipon et al. (hereinafter Tipon) under 35 U.S.C. § 103.

The Examiner states that all the features of claim 1 of the instant application are disclosed by Hess except for a connection of the hardware arithmetic-logic unit with at least one table memory. The Examiner relies on Tipon to teach this last feature. Applicant respectfully disagrees and now presents his arguments.

The method claim 1 of the instant application requires the

step of:

> accessing the table memory with the digital processor by taking the preselected base address as a starting point for computing, according to a prescribed arithmetic computation rule in hardware, a plurality of addresses used for consecutive read access operations and/or consecutive write access operations in the table memory.

Fig. 1 of Tipon shows an offset addressing unit, wherein a processor 12 accesses a base address register 18. According to the Office Action, the Examiner identifies the base address register 18 with the table memory of claim 1 (see Examiner's comments on page 4, lines 11-17 of the Office Action). Moreover, the Examiner identifies the plurality of addresses required by claim 1 of the instant application with addresses computed by the arithmetic logic unit 24 (see Examiner's comments on page 4 of the Office Action).

According to claim 1 of the instant application, the plurality of addresses is used for read and/or write access in the memory table. This feature would only be disclosed in Tipon if the addresses computed by the arithmetic logic unit 24 were to be used for a read and/or write access in the base address register 18. However, this is not disclosed by Tipon, since the addresses are exclusively forwarded to an external memory device and an external bus system (see the right hand side of Fig. 1

stating, "TO MASS STORAGE MEMORY" and "TO/FROM MAIN MEMORY ADDRESS BUS").

A similar argumentation holds for the corresponding independent device claim 11 of the instant application, which requires:

> a hardware address computation circuit for, taking the base address as a starting point, applying an arithmetic computation rule to produce a plurality of addresses enabling the digital processor to consecutively access said table memory.

This feature would only be disclosed in Tipon if the arithmetic logic unit 24 (identified as the hardware address computation circuit) produces addresses enabling the digital processor 12 to access the base address register 18 (identified as table memory). However, since the addresses are exclusively forwarded to a memory device and a bus system (see comments above), the digital processor 12 is not enabled to access the base address register 18 by using the computed addresses. Accordingly, it is respectfully stated that the cited feature is not disclosed by Tipon.

Method claim 2 of the instant application requires the storage of *"a plurality of base addresses associated with a plurality of different data types"* and a preselection of *"the base address by using the processor to set a*

selection bit associated with the base address". The Examiner alleges the subject matter of claim 2 to be disclosed in column 6, lines 6 to 17 of Tipon. In the cited text passage, Tipon refers to Fig. 2 and discusses the structure of the used 32-bit address 80. Moreover, an examination of contained (overlap) bits by the page displacement circuit 56 to determine current page accesses (see column 6, lines 17 to 24) is discussed in this text passage. Neither the cited text passage nor the rest of the document discloses the storage of different data types or the usage of a selection bit. A similar argumentation holds for the corresponding device claim 12 of the instant application.

Claim 3 of the instant application teaches *"prescribing the plurality of base addresses unalterably in hardware".* In contrast, Tipon explicitly suggests the loading of the base address register 18 by the processor 12, with the loading of a base address being performed according to a computer program (see column 3, lines 22 to 29). Consequently, the base addresses are not prescribed in hardware and the subject matter of the claim 3 is not believed to be disclosed.

Further, the Examiner alleges Tipon teaches the subject

matter of the claim 8 of the instant application which recites "*providing a second data type as trace back values…*" and "*the digital processor programming how many states the trace back values need to include*". In this context the Examiner refers to Fig. 1 and sees the cited features disclosed therein. In our opinion, it is obvious that Fig. 1 does not provide any information on used data types or any logic implementations of the digital processor 12. Moreover, we believe that these features are also not disclosed in the rest of the document.

Claim 20 of the instant application requires the hardware arithmetic-logic unit to include an equalizer hardware arithmetic-logic unit and a decoder hardware arithmetic-logic unit. The Examiner alleges these features are disclosed in Fig. 1 of Tipon. This appears to be in contradiction to the Examiner's analysis provided in relation to independent claims 1 and 11 in Office Action, where the Examiner argued that the hardware arithmetic-logic unit is disclosed by Hess, instead of Tipon. In Tipon, the Examiner fails to identify any hardware arithmetic-logic unit. Therefore, the reasoning of the Examiner, in view of claim 20 is respectfully not understood.

In item 8 on pages 7-8 of the above-identified Office Action, claim 7 has been rejected as being obvious over U.S. Patent No. 4,405,980 to Hess (hereinafter Hess) in view of U.S. Patent No. 5,150,471 to Tipon et al. (hereinafter Tipon) and further in view of U.S. Patent No. 3,833,888 to Stafford et al. (hereinafter Stafford) under 35 U.S.C. § 103.

The Examiner alleges that the subject matter of the claim 7 of the instant application is disclosed by Stafford and in this regard refers to the Abstract of Stafford. Stafford is not believed to disclose (neither in the abstract nor in the rest of the document) the usage of channel decoding or any specifications on logic implementations of the digital processor, thereby determining how many soft input values per unit time can be stored. Thus the subject matter of claim 7 is cannot be disclosed by Stafford.

In item 9 on pages 8-9 of the above-identified Office Action, claims 9-10 have been rejected as being obvious over U.S. Patent No. 4,405,980 to Hess (hereinafter Hess) in view of U.S. Patent No. 5,150,471 to Tipon et al. (hereinafter Tipon) and further in view of U.S. Patent No.

6,310,891 to Dove et al. (hereinafter Dove) under 35 U.S.C. § 103.

Claim 9 of the instant application recites "*choosing a packing mode causing a plurality of data words, output by the processor for performing the step of accessing the table memory, to be combined to form a memory data word for the table memory*". The Examiner finds the subject matter of claim 9 to be disclosed by Dove. Dove concerns a method of scheduling a plurality of time multiplexed cells and a plurality of asynchronous cells in a temporal frame. The concrete structure of the temporal frame is illustrated in Fig. 1. However, Dove does not disclose a processor outputting data words to be packed and a table memory for which the combined data word is provided. A similar argumentation is valid for claim 10, which requires the choice of an unpacking mode.

In item 10 on pages 9-11 of the above-identified Office Action, claims 16-17 have been rejected as being obvious over U.S. Patent No. 4,405,980 to Hess (hereinafter Hess) in view of U.S. Patent No. 5,150,471 to Tipon et al. (hereinafter Tipon) and further in view of U.S. Patent No. 6,363,119 to Oami (hereinafter Oami) under 35 U.S.C. § 103.

Claim 16 of the instant application recites "*a multiplexer and buffer device for assembling a plurality of data words output by said processor to form a memory data word intended for being stored at an address in said table memory*". The Examiner asserts that the subject matter of claim 16 is disclosed by Oami, thereby citing column 25, lines 51 to 61, in connection with Fig. 5. Fig. 5 shows a multiplexer 95 receiving data from an arithmetic coding section 91 (identified as processor), which is, stored in a buffer of the multiplexer 95. However, Oami does not disclose the formed data (identified as enhancement layer bit-stream, see right hand side of Fig. 5) to be intended for being stored in a table memory. A similar argumentation is valid for claim 17 of the instant application, which contrarily requires the usage of a multiplexer (see Fig. 4 concerning this matter).

In item 11 on page 11 of the above-identified Office Action, claim 19 has been rejected as being obvious over U.S. Patent No. 4,405,980 to Hess (hereinafter Hess) in view of U.S. Patent No. 5,150,471 to Tipon et al. (hereinafter Tipon) and further in view of U.S. Patent No. 5,311,523 to Serizawa et al. (hereinafter Serizawa) under 35 U.S.C. § 103.

Claim 19 ultimately depends from claim 11, and since claim 11 is believed to be allowable for the above-stated reasons, claim 19 is also believed to be allowable.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 1 or 11. Claims 1 and 11 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1 or 11.

In view of the foregoing, reconsideration and allowance of claims 1-20 are solicited.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account

of Lerner Greenberg Stemer LLP, No. 12-1099.

Respectfully submitted,

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